

**REMARKS**

Claims 1-7 are pending. Claims 1 and 7 are the only independent claims and have each been amended. Claim 1 has been amended merely to improve its form, without narrowing its scope.

Applicant thanks the Examiner for the indication that claim 7 would be allowed if rewritten in independent form. Since that claim has been so rewritten, it is now believed in condition for allowance.

In the Office Action, the specification was again objected to on the grounds that DATA#0 and DATA#1 of Figure 1 are not in the specification. However, the specification was amended in the previous response to address this informality. Withdrawal of the objection is requested.

Claims 1-6 were rejected under 35 U.S.C. § 103 over U.S. Patent 6,728,271 (Kawamura et al.) in view of U.S. Patent Publication No. 2004/0160898 (Lim et al.). Applicant traverses and submits that independent claim 1 is patentable over the cited art for at least the following reasons.

Claim 1 is directed to a packet processing circuit including: a plurality of macros each of which processes packet data on the basis of a clock and outputs the processed packet data from at least one route, the macros being cascade-connected; and a clock supply unit which supplies the clock to a macro to be controlled and, when no packet data is output for a predetermined time from all routes of a macro located at an input side of the macro to be controlled, stops supplying the clock to the macro to be controlled.

In the circuit defined in claim 1, a clock supply unit stops supplying a clock to a macro being controlled when no packet data is output from all routes of a macro that is located at the input side of the macro being controlled. In claim 1, the "macro to be controlled" (macro 1) and the "macro located at an input side of said macro to be controlled" (macro 2) are two different macros that are part of a plurality of cascade-connected macros. Macro 2 is a macro located at the input

side of macro 1. In claim 1, whether or not a clock is supplied to macro 1 is decided based upon whether packet data has been output from macro 2 for a predetermined period of time.

Kawamura teaches stopping a clock signal. However, Kawamura does not teach or suggest cutting off the clock in the same manner, or under the same circumstances, as recited in claim 1. Kawamura relates to a stream demultiplexing device that can extract multiplexed data in payloads of received transport packets. The payload processor extracts data from current transport packet and stores the extracted data into a data storage corresponding to the stream to which the data belongs.

In Kawamura, according to the portion of the patent cited by the Examiner, the clock signal is stopped *to the payload processing unit* once this payload processing unit finishes storing the data for a particular transport packet. In view of this reliance, the position is being taken in the Office Action that the payload processing unit is the element of Kawamura that corresponds to the “macro to be controlled,” since this element is the element of claim 1 to which the clock supply is stopped.

However, in claim 1, the decision as to when the clock is to be stopped to the “macro to be controlled” is based on what occurs in relation to *a different macro*, namely the “macro located at an input side of said macro to be controlled.” In contrast, as is made clear in col. 2, lines 16-22 in Kawamura, whether to stop the clock signal to the payload processing unit is based upon actions of the payload processing unit itself (i.e., the fact that *it* has finished transferring the data portion), not upon a predetermined period of time since *a different element* has output a packet. In summary, in Kawamura, when the clock signal is stopped is based upon the actions of the payload processing unit itself, and not of a unit located at an input side of the payload processing unit.

Moreover, contrary to the position repeated in the Office Action, Lim does nothing to cure the above-mentioned deficiency of Kawamura as a reference against claim 1. Even if Lim were to be deemed, for purposes of argument, to teach all it is cited for, it does not remedy the deficiency that in Kawamura it is the actions of the payload processing unit, the very element being

controlled by the stopping of the clock, that cause the clock to be stopped. For at least this reason, even if Kawamura and Lim were to be combined, they would not teach or suggest all the elements of claim 1. For at least this reason, claim 1 is believed clearly patentable over the cited combination.

Moreover, in Lim, power on for a module is performed when Ethernet handshaking signals indicate that a packet is arriving. Each module is provided with a logic circuit that monitors the handshaking signals provided to that module. If the handshaking signals indicate a packet is about to be transmitted to that module, power up of that module is performed.

Subsequent power down of the module is performed automatically when the entire packet has been transferred from the module. For example, as discussed at paragraph [0024], a logic circuit in the MAC-RX (Figure 1) controls that module to power down automatically when the entire packet has been transferred to the corresponding RX module. However, this power reduction method does not meet the above-mentioned limitation of claim 1 relating to the clock supply unit, which supplies the clock to a macro to be controlled and, when no packet data is output for a predetermined time from all routes of a macro located an input side of the macro to be controlled, stops supplying the clock to the macro to be controlled.

The Office Action, at page 7, states that “referenced section 0031” has not been considered by the Applicant. This is incorrect, as was pointed out in the previous response, paragraph [0031] discusses an alternative embodiment in which modules “remain powered up even after they have finished transmitting any packet(s) within them.” However, even if a module in Lim powered up a predetermined amount of time after it transmits a packet within it, this does not correspond to the recited feature of the clock supply unit. The clock supply unit of claim 1 controls application of a clock signal to a particular macro (the macro to be controlled), not on the basis of whether that macro (i.e., the macro to be controlled) has transmitted a packet within it, but based on whether packet data has been output from *a macro located at an input side* of the macro to be controlled.

As was pointed out in the previous response, in both the embodiment disclosed in Lim's paragraph [0024] and in the embodiment shown in Lim's paragraph [0031], power down of a module is based upon what the module has done with a packet within it, whether this is done immediately upon transmitting the packet (as in Lim's paragraph [0024]), or a predetermined time afterward (as in Lim's paragraph [0031]). This is quite different that what is recited in claim 1, in which the clock supply unit, which supplies the clock to a "macro to be controlled," stops supplying the clock to the macro to be controlled when no packet data is output for a predetermined time from all routes of a "macro on an input side of the macro to be controlled."

As to the portions of Lim quoted at page 8 of the Office Action, these portions do not say that the clock is turned off on the basis of a determination that no new packet is expected, as the Examiner seems to be implying. In the embodiment under discussion in paragraphs [0024] to [0026], the power down state is always entered after the packet has been transmitted, *unless there is a new incoming packet* detected by Check Activities state 15. That is, state 13 (power on) is entered upon receipt of a handshake signal that a packet is about to be received. Upon the packet having been transmitted, the system passes back to state 11 (power down) unless check 15 determines that a new packet is about to be received. Thus, power down (stopping the clock signal) is performed *based upon the transmission of the packet*, even though proceeding to the power down state may be delayed if an incoming packet is detected.

For this additional reason, even if the reference were to be combined, they would not meet the features of claim 1.

Moreover, one of ordinary skill in the art would not have applied the power reduction techniques of Lim to Kawamura. In Kawamura the periods during which the clock is not supplied are based on activities and data receipt related to Kawamura's demultiplexing function. For example, the clock signal is stopped in Kawamura when the data for the current transport packet has been safely stored in its appropriate storage location. Substituting other power reduction techniques, such as those discussed in Lim, into the Kawamura system would change the principle of operation of Kawamura, and not take into account the reason Kawamura selects the time periods

it does, i.e., in accordance with events occurring during the demultiplexing process. Thus, there would also be no reason to make the proposed combination.

For at least the above reasons, independent claim 1 is believed patentable over the cited references, taken individually or in combination. The other claims are dependent upon claim 1 and are patentable for at least the same reasons.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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